Dr. SHAHANA T.K.
Professor
Division of Electronics Engineering
School of Engineering
Cochin University of Science and Technology
Kochi - 682 022, India
Phone: 9895839629
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Objective:

To excel in teaching and research activities in the field of Digital VLSI Design and reconfigurable architectures for wireless communication systems

Educational Qualifications:

Ph. D in Electronics
Thesis Title: **EFFICIENT TRANSMITTER/RECEIVER ARCHITECTURES FOR HIGH PERFORMANCE WIRELESS APPLICATIONS**
Department of Computer Science
Cochin University of Science and Technology (2009)

M.Tech Electronics
Specialization: Digital Electronics
Cochin University of Science and Technology (1999)
Score: 80.8%, CGPA: 3.24/4 - First class with Distinction

B. Tech Electronics and Communication
M.A. College of Engineering, Kothamangalam
Mahatma Gandhi University (1997)
Score: 85.6% - First class with Distinction and Third Rank

Academic Honours/Scholarships:

Received Third Rank for B. Tech Degree in Electronics and Communication of Mahatma Gandhi University in 1997.

GATE Scholarship of UGC for a period of One and Half Years (1997-1999) during M.Tech

Best paper award for the paper Effect of Active Layer Thickness Variation on Overlap Length Scaling in a-IGZO Thin Film Transistors presented in 2021 8th International Conference on Smart Computing and Communications (ICSCC), 2021 by Roshna B. Raj, A. Tripathi, S. Nair, D. Gupta, T. K. Shahana and T. Mukundan.

TCS Best Student Project Award-2016, by Tata Consultancy Services for The final year B.Tech major project titled "Robotic Arm" by John K.G., Anjana R. Krishnan, Gatha S. Manohar, Anjali A.V., and Arathy J under the guidance of Dr Shahana T.K.

Work Experience:

23 years of teaching experience from 25-02-1999 onwards as faculty in Division of Electronics Engineering, School of Engineering, Cochin University of Science and Technology.

Designation	Duration from- to dates
Professor	23-5-2015 onwards
Associate Professor	23-5-2012 to 22-5-2015
Reader	24-6-2009 to 22-5-2012
Lecturer (Selection grade)	23-5-2009 to 23-6-2009
Lecturer (senior scale)	23-5-2004 to 22-5-2009
Lecturer	25-2-1999 to 22-5-2004

Research Areas:

- Multi-standard Wireless Designs
- VLSI System Design, Micro-electronics
- Communication Systems

**Produced 1 PhD, submitted 2 PhD theses and presently guiding 6 PhD students

Participated/Presented papers/Session chaired in International / National Conferences including:

- IEEE 67th Vehicular Technology Conference: VTC2008-Spring, Singapore, 11–14 May 2008.
- IET International Conference on Information and Communication Technology in Electrical Sciences (ICTES 2007), Chennai, India, 20-22 December 2007.
- National Conference on Broadband Technologies (Broadband 08), organized by MBCET Trivandrum in association with IEEE Kerala section and CSI Trivandrum chapter, March 2008.
- International Conference on Information and communication Techniques, ICICT 2014, organized by SOE, CUSAT, under TEQIP from Dec 3-5, 2014.
- 8th International Symposium on Embedded Computing and system Design (ISED 2018), organized by Department of Electronics, CUSAT, India, 13-12-2018 to 15-12-2018
- International Conference on Digital Pedagogies: Changing Mindsets for Sustainable Learning, AICTE Auditorium, New Delhi, India, 1-4-2019 to 3-4-2019

Reviewer of various International journals, Reviewer and Session Chair for National and International conferences

Publications:

International Journal : 25

Book Chapters : 1

International conference : 46

National conference : 4

(List appended)

Research Projects undertaken:

SI No	Title	Funding Agency	Amount & Duration	Designation
1.	System level Analysis and Design of Reconfigurable Multistandard Sigma-Delta ADCs for Next Generation Wireless Transceivers*	KSCSTE	10.29 Lakhs 2013-16	Co-Investigator
2.	Design and Optimization of Organic Thin Film Transistors	TEQIP Seed Money Project	2018-2019 1 Lakh	Principal Investigator

*The project was ranked **Grade – 'A' (Excellent)** by the Research Council for Engineering and Technology Programme (RC-ETP).

Co-ordinator:

AICTE sponsored Staff Development Programme on *System level Modeling, Design and Analysis – A Practical Approach* conducted at Division of Electronics Engineering, School of Engineering, CUSAT, from 6-6-2011 to 17-6-2011

Other Responsibilities Carried out:

Head of the Division	Division of Electronics Engg, SoE, CUSAT	26 April 2019- 3 May 2020
Member, BOS	Board of studies in EEE/EC, CUSAT	23.10.2019 for a period of 4 years
Member, Industry Institute Interaction Cell	SOE, CUSAT (Under TEQIP Phase III)	2017 and Ongoing

Faculty Co-ordinator	ECSA, Electronics and Communication Students Association	2012-2013, 2018-19, 2021-22
Class Co-ordinator	2000, 2004, 2010, 2015 and 2018 B.Tech, admissions	2000-2004, 2004-2008, 2010-2014, 2015-2019 and 2020-2022
Editor	Proceedings of AICTE SDP on *System level Modeling, Design and Analysis – A Practical Approach*, Division of Electronics Engineering, SOE, CUSAT, 06.06.2011 – 17.06.2011	2011
Committee Member, CASH	Committee Against Sexual Harassment (CASH) of SOE	Since 2016
Doctoral Committee Member	in Electronics and Communication Engineering of APJ Abdul Kalam Technolological University	Since 2016
Member	Anti-ragging squad of SOE	2015-2016, 2016-2017
Staff in charge	Microprocessor Lab, EC Division	Since 2006
Member, organizing committee	ISTE STTP on 'Modelling and Optimization Techniques in Engineering', 2010, Division of Electronics Engineering, 2012 International Conference on Data Science & Engineering (ICDSE), Department of Computer Science, CUSAT, "International Conference on Information and communication Techniques, ICICT 2014", organized by SOE, National Workshop on Technology for Aged (NWTA), 2015, International Conference on Recent trends in Engineering and Technology organized by SOE, 2016	
Question paper setter, Examiner, Chief examiner, External examiner and Passing board member for PG and UG	Several undergraduate and post graduate examinations conducted by CUSAT	Since 1999

Membership in Professional bodies:

Life Member – Indian Society for Technical Education (ISTE)
Fellow Member – Institute of Electronics and Telecommunication Engineers (IETE)
Life Member - Indian Society of Systems for Science & Engineering (ISSE)

Personal Details:

Age & Date of Birth	**: 45 years, 21-05-1976**
Gender	**: Female**
Marital status	**: Married**
Nationality	**: Indian**
Permanent Address	**: MNRA 50, Kizhakkechela veedu Cross Road - 4, Maveli Nagar Cochin University P.O., Kochi -682 022**

Declaration:

I hereby declare that the information furnished above is true to the best of my knowledge.

Dr. SHAHANA T.K.

LIST OF PUBLICATIONS

International Journals:

1. Pramod P. and **Shahana T.K**., "High Throughput and Energy Efficient Linear Phase FIR Filter Architectures", *Microprocessors and Microsystems, ELSEVIER*, Volume 87, November 2021, 104367. https://doi.org/10.1016/j.micpro.2021.104367
2. Preenu Paul, Babita R. Jose, **T. K. Shahana**, Chikku Abraham, and Jimson Mathew. "High Gain Isolated Quasi Switched Boost Converter Embedded with Switched Capacitor Cell" *Electric Power Components and Systems, Taylor and Francis, SCIE Journal,* 49:4-5, 333-344,16 October 2021(published online), https://doi.org/10.1080/15325008.2021.1971334
3. Roshna, B. Raj, Ashutosh Kumar Tripathi, Pradeep Kumar Mahato, Shiny Nair, **T. K. Shahana**, and T. Mukundan. "Effect of active layer thickness variation on scaling response in a-IGZO thin film transistors under Schottky limited operation." *Semiconductor Science and Technology (2021)*. IOP Publishing, August 2021. https://doi.org/10.1088/1361-6641/ac1d62. Impact Factor 2.361 (SCIE).
4. V. V. Mahesh, **T K Shahana**, "Design and synthesis of filter bank structures based on low order constrained least square and minimum phase methods for audiogram matching in digital hearing aids," *Health and Technology, Springer,* Published on 09/11/20 (online), doi: 10.1007/s12553-020-00496-5
5. Jithendra.K.B, **Shahana.T.K** "New Results in Biclique Cryptanalysis of Full Round GIFT", Journal of Intelligent and Fuzzy Systems, IOS Press, 41 (2021) 5551-5560, DOI:10.3233/JIFS-189875 (SCI Impact Factor 2020 - 1.851)
6. Jithendra.K.B, **Shahana.T.K**, "New results in Reduced Round AES-256 Impossible Differential Cryptanalysis" International Journal of Computing and Digital Systems" , Vol. 9, No.4, July 2020, pp. 755-764 (SCOPUS)
7. Jithendra.K.B, **Shahana.T.K**, "ACT: An Ultra-Light Weight Block Cipher For Internet of Things", International Journal of Computing and Digital Systems" 2020, Vol. 9 No.5 pp-921-929 (SCOPUS)
8. Pramod P. and **Shahana T.K**., "An efficient architecture for signed carry save multiplication", ***IEEE letters of computer society***, Vol. 3, No. 1, pp.9-12, January–June 2020.
9. P. Pramod and **T.K. Shahana**, "Efficient modular hybrid adders and Radix-4 booth multipliers for DSP applications", ***Microelectronics Journal, Elsevier***, January 2020, Print ISSN 0026-2692, https://doi.org/10.1016/j.mejo.2020.104701. H-index-59, Science Citation Index (SCI) Expanded
10. Pramod P., and **Shahana T. K**., " Delay and Energy Efficient Modular Hybrid Adder for Signal Processor Architectures", ***IETE Journal of Research***, Taylor & Francis, Print ISSN:0377-2063, OnlineISSN: 0974-780X, 23 June 2019, https://doi.org/ 10.1080/03772063.2019.1627917 [SCIe indexed, impact factor 0.829]
11. Pramod P., and **Shahana T. K**., "High Throughput FIR Filter Architectures Using Retiming and Modified CSLA Based Adders" ***IET Circuits, Devices and Systems***, Print ISSN 1751-858X, Online ISSN 1751-8598, https://doi.org/10.1049/iet-cds.2019.0130 Volume 13, Issue 7, October 2019, pp. 1007 – 1017 [SCI indexed, impact factor 1.319]

12. Rijo Sebastian, Jos Prakash, Babita Roslind Jose, **Shahana T.K**, Jimson Mathew, "A re-configurable MASH 2-2 bandpass DQEFM for multi-standard applications", ***International Journal of Electronics***, Taylor and Francis. April 2019, Vol.106, Issue 10, pp. 1498-1513, https://doi.org/10.1080/00207217.2019.1600737 [SCI indexed, impact factor 1.070]
13. Pramod, P., **Shahana, T.K**., "High throughput adaptive filter architecture using modified transpose form FIR filters", ***Journal of Advanced Research in Dynamical and Control Systems***, vol.10, no.15, pp. 68-82, Nov. 2018. [SCOPUS SJR, H index 8]
14. Jithendra.K.B, **Shahana.T.K**, "A Novel Approach in Substitution for Reduced Complexity and Better Cryptographic Strength of AES. " ***Journal of Advanced Research in Dynamical and Control Systems***, vol.10, no.15, pp. 183 - 191, Nov. 2018. [SCOPUS SJR, H index 8]
15. Mahesh V V, **Shahana T K** ,"Constrained least square nonuniform dynamic filter bank for delay and Hardware efficient digital hearing aids", ***Health and Technology, Springer*****,** 30 Oct 2018, Vol 9, Issue 3, pp 355–363 print ISSN 2190-7188, online ISSN 2190-7196, https://doi.org/10.1007/s12553-018-0268-9 [SJR 0.28, H index 12]
16. Rijo Sebastian, Jos Prakash, Babita Roslind Jose, **Shahana T.K**, "Multi-Stage Noise Shaping ΔΣ Modulator with Enhanced Noise Shaping for Low Power Wideband Applications". ***Journal of Low Power Electronics***, Volume 13, Number 4, December 2017, pp. 661-668(8). [ESCI, SCOPUS]
17. Rijo Sebastian, Babita Roslind Jose, **Shahana T.K**, Jimson Mathew "A Low-distortion Hardware Efficient MASH Sigma Delta Modulator with Enhanced Noise Shaping" ***Journal of Smart Science, (Taylor and Francis)***, Vol.6, issue 2, pp.158-172, Published online: 22 Dec 2017. doi.org/10.1080/ 23080477.2017.1417962 [ESCI, SCOPUS]
18. Jithendra K.B. and **Shahana T.K.**, "Embedded Low Hardware Parallel Data Integrity Verification for Block Ciphers", ***ISTP Journal of Research in Electrical and Electronics Engineering*** **(ISTP-JREEE)**, pp. 193-197, August 2014.
19. **Shahana T. K.**, Babita R. Jose, K. Poulose Jacob and Sreela Sasi, "A Novel Sigma-Delta based Parallel Analog-to-Residue Converter", ***International Journal of Electronics,*** Taylor and Francis Ltd., Vol. 96, Issue 6, pp. 571 – 583, June 2009.
20. **Shahana T. K.**, Babita R.Jose, K.Paulose Jacob and Sreela Sasi, "Decimation Filter Design Toolbox for Multistandard Wireless Transceivers using MATLAB", ***International Journal of Signal Processing***, World Academy of Science, Engineering and Technology, Vol. 5, No. 2, pp. 154-163, Spring 2009.
21. **Shahana T. K.**, Babita R. Jose, Rekha K. James, K. Poulose Jacob and Sreela Sasi, "RNS based Programmable Decimation Filter for Multi-Standard Wireless Transceivers", ***ECTI Transaction on Electrical Engineering, Electronics and Communications***, ECTI – Transaction Journal, Vol. 6, No. 2, pp. 57-66, 2008. [SCOPUS, ACI]
22. **Shahana T. K.**, Babita R. Jose, Rekha K. James, K. Poulose Jacob and Sreela Sasi, "A Toolbox Approach to Decimation Filter Design for Multi-Standard Wireless Transceivers", ***IETECH Journal of Communication Techniques,*** *International Engineering and Technology Publications*, Vol.2, No.3, pp. 181-188, 2008.
23. **Shahana T. K.**, Babita R. Jose, K. Poulose Jacob and Sreela Sasi, "RRNS-Convolutional Concatenated Code for OFDM based Wireless Communication with Direct Analog-to-Residue Converter", ***International Journal of Electrical, Computer and Systems Engineering***, World Academy of Science, Engineering and Technology, Vol. 2, No. 2, pp.86-93, Spring 2008.
24. Babita R. J., **Shahana T. K.**, P. Mythili and J. Mathew, "Sigma-Delta Analog to Digital Converter for WLAN with RNS based Decimation Filter", ***IETECH Journal of Information Systems***, *International Engineering and Technology Publications*, Vol. 2, No. 2, pp. 68-75, 2008.

Book Chapter:

25. V. V. Mahesh, T K Shahana "Design and synthesis of filter bank structures based on constrained least square method using hybrid computing for audiogram matching in digital hearing aids", Sustainable Intelligent Systems, Advances in Sustainability, Science and Technology, Springer, pp. 215- 234, 2021, ISBN:978-981-334-901-8 https://doi.org/10.1007/978-981-33-4901-8_13

International Conferences:

26. Roshna B. Raj, A. Tripathi, S. Nair, D. Gupta, **T. K. Shahana** and T. Mukundan, "Effect of Active Layer Thickness Variation on Overlap Length Scaling in a-IGZO Thin Film Transistors," 2021 8th International Conference on Smart Computing and Communications (ICSCC), 2021, pp. 319-322, doi: 10.1109/ICSCC51209.2021.9528296.
27. B. K. Jeemon and **Shahana T.K**, "Space Time Block Coded Vector OFDM with ML Detection," 2021 8th International Conference on Smart Computing and Communications (ICSCC), 1-3 July 2021, pp. 145-148, doi: 10.1109/ICSCC51209.2021.9528236.
28. Basil K Jeemon, **Shahana T K**, "Design and Analysis of a Novel Space-Time-Frequency Block Coded Vector OFDM Scheme Robust to Rayleigh Fading", 17th IEEE India Council International conference (INDICON 2020), 11th-13th Dec 2020.
29. V.V. Mahesh, **T. K. Shahana**, "Design and synthesis of Filter Banks using area and power efficient stochastic computing," IEEE World conference on smart trends in systems, security and sustainability 2020, London, pp. 662-666, July 2020 doi: 10.1109/WorldS450073.2020.9210403
30. Raj, Roshna B., Shiny Nair, Ashutosh Tripathi, T. Mukundan, and T. K. Shahana. "Influence of active layer thickness on the cut-off frequency of a-IGZO thin film transistors" In *Journal of Physics: Conference Series*, vol. 1495, no. 1, p. 012016. IOP Publishing, 2020.
31. Pramod P. and **Shahana T.K.,** "High throughput and energy efficient FIR filter architectures using retiming and two level pipelining", Third International Conference on Computing and Networking Communications (COCONET), Thiruvananthapuram, 18-20 December 2019.
32. Preenu Paul, Babita R Jose, **Shahana T.K**., Chikku Abraham, Jimson Mathew, "Isolated Switched Boost DC-DC Converter with Coupled Inductor and Transformer",TENCON 2019,IEEE Region 10 conference at Grand Hyatt Kochi Bolgatti, Kerala, India, 17-20 October 2019.
33. Jithendra.K.B, **Shahana.T.K**, " A New Efficient Sbox for Strengthening PRESENT Like Block Ciphers Against Linear Cryptanalysis", 2nd International Conference On Intelligent Computing, Instrumentation And Control Technologies (ICICICT-2019), Kannur July 2019 IEEE Xplore
34. Jithendra.K.B, **Shahana.T.K**, " New Biclique Cryptanalysis on Full Round PRESENT- 80 Block Cipher", International Conference on Adaptive Computational Intelligence (ICACI-2019) Mysore, July 2019, Institution of Electronics and Telecommunication Engineers Springer
35. Rijo Sebastian, Jos Prakash, Babita Roslind Jose, **Shahana T.K**., Jimson Mathew, "Lowpass MASH DQEFM for 4G wireless receivers", *7th International Conference on Smart Computing &* Communications (ICSCC 2019), Curtin University, Malaysia during 28-30 June 2019.
36. Roshna, B. R., **T. K. Shahana**, and Shiny Nair. "Threshold voltage engineering in a-IGZO thin film transistors through active layer doping and thickness control" AIP Conference Proceedings. Vol. 2082. No. 1. AIP Publishing,January 2019.

37. Jithendra.K.B and **Shahana.T.K**, "New Results in Related Key Impossible Differential Cryptanalysis on Reduced Round AES-192", IEEE *Int. Conf. on Advances in Communication and Computing Technology (ICACCT),* Sangamner, India, February 2018, pp 291-295.
38. Rijo Sebastian, Jos Prakash A.V., Babita Roslind Jose, **Shahana T.K**., "A multi-mode MASH ΣΔ Modulator for low power wideband applications", 6th International Symposium on Embedded Computing and System Design (ISED 2016) held at IIT Patna, 15-17 Dec 2016 (Conference proceedings at IEEE digital Xplore).
39. Mahesh V.V., **Shahana T.K**. "Delay and Area Efficient Sound Wave Decomposition by Nonuniform Filter Bank for Digital Hearing Aids," Proceedings of SAI Intelligent Systems Conference (IntelliSys) 2016. IntelliSys 2016. Lecture Notes in Networks and Systems, vol 15. Springer, Cham. https://doi.org/10.1007/978-3-319-56994-9_5
40. Jithendra K.B., **Shahana T.K.** "Elastic Serial Substitution Box for Block Ciphers with Integrated Hash Function Generation," Proceedings of SAI Intelligent Systems Conference (IntelliSys) 2016. IntelliSys 2016. Lecture Notes in Networks and Systems, vol 16. Springer, Cham. https://doi.org/10.1007/978-3-319-56991-8_48
41. Rijo Sebastian, Babita Roslind Jose, **Shahana T.K.**, **"**GA based Optimization of Second Order ΣΔ Modulator for Digital Hearing Aid Applications", ***Proceedings of 4th International Conference on Eco-friendly Computing and Communication Systems, ICECCS 2015, Elsevier Procedia Computer Science 70 (2015)*** 274 – 281, organized by National Institute of Technology, Kurukshetra, 7- 8 December 2015.
42. Jithendra.K.B, **Shahana.T.K**, "Enhancing the uncertainty of Hardware Efficient Substitution Box based on Differential Cryptanalysis", *Proceedings of* ***Fourth International Conference on Advances in Signal Processing and Communication*** *(Walter De Gruyter- Germany)*, Trivandrum, 30-31 October 2015
43. Rijo Sebastian, Babita Roslind Jose, **Shahana T.K., "**An Optimized High Resolution ΣΔ Modulator for Digital Hearing Aid Applications", ***Proceedings of Fifth International Workshop on Advances in Computing and Communications***, organized by Rajagiri School of Engineering and Technology, pp. 144-147, 2015.
44. Jithendra.K.B, **Shahana.T.K**, "High Security Pipelined Elastic Substitution Box with Embedded Permutation Facility", *Proceedings of Second International Conference on Innovations in Computer Science and Engineering. Springer Science+Business Media Singapore Advances in Intelligent Systems and Computing* 413, Hyderabad, pp. 79-86, 7-8 August 2015.
45. Jithendra.K.B, **Shahana.T.K**, "Enhancing the uncertainty of Hardware Efficient Substitution Box based on Linear Cryptanalysis", *Proceedings of Fifth International Conference on Computational Intelligence and Information Technology, Walter De Gruyter- Germany*, Bangalore, pp. 265-272, 1st August 2015
46. Jithendra K.B. and **Shahana T.K.**, "High Security Elastic Serial Substitution Box for Block Ciphers", Proc. of 2nd International Conference on Networking, Information and Communications, ICNIC 2015, organized by Sri Venkateshwara College of Engineering, Bengaluru, India, 18-20 May 2015.
47. Roshna B. Raj and **Shahana T.K.**, "Effect of SRAM Power Optimization Techniques on Performance and Reliability", Proc. of 2nd International Conference on Networking, Information and Communications, ICNIC 2015, organized by Sri Venkateshwara College of Engineering, Bengaluru, India, during 18-20 May 2015.
48. Anas Muhammed. A. K, Jayakrishnan K.R. and **Shahana T. K.**, "Delta Sigma Modulator in 90nm using Modified Op-Amp and Latched comparator", 2nd International Conference on Emerging Trends in Technology and Applied Sciences, ICETTAS'15, organized by SAINTGITS College of Engineering, Kottayam, Kerala on 30th April, 1st and 2nd May 2015.

49. Anjali Suresh, Jayakrishnan K.R. and **Shahana T. K.**, "Operational Amplifier Design for Delta- Sigma Modulators", 2nd International Conference on Emerging Trends in Technology and Applied Sciences, ICETTAS'15, organized by SAINTGITS College of Engineering, Kottayam, Kerala on 30th April, 1st and 2nd May 2015.
50. Bobby Thomas, Jayakrishnan K.R. and **Shahana T. K.**, "Fully Differential Op-amp Design For Wide band Continuous Time Delta Sigma Modulators", 2nd International Conference on Emerging Trends in Technology and Applied Sciences, ICETTAS'15, organized by SAINTGITS College of Engineering, Kottayam, Kerala on 30th April, 1st and 2nd May 2015.
51. Pinka Abraham, Jayakrishnan K.R. and **Shahana T. K.**, "Comparator Design for Delta Sigma Modulator", 2nd International Conference on Emerging Trends in Technology and Applied Sciences, ICETTAS'15, organized by SAINTGITS College of Engineering, Kottayam, Kerala on 30th April, 1st and 2nd May 2015.
52. Remya Thankachan, Jayakrishnan K.R. and **Shahana T. K.**, "Design of 1-bit DAC for Delta-Sigma Modulator", 2nd International Conference on Emerging Trends in Technology and Applied Sciences, ICETTAS'15, organized by SAINTGITS College of Engineering, Kottayam, Kerala on 30th April, 1st and 2nd May 2015.
53. Jithendra K.B. and **Shahana T.K.**, "Hardware Efficient Parallel Substitution Box for Block Ciphers with Static and Dynamic Properties", Elsevier Procedia Computer Science 46 (2015), Proc. of International Conference on Information and communication Techniques, ICICT 2014, organized by SOE, CUSAT, under TEQIP, pp. 540-547, Dec 3-5, 2014.
54. Jayakrishnan K.R. and **Shahana T. K.,** "Excess Loop Delay Mitigation Techniques in Wideband Continuous Time Delta-Sigma Modulators", ***International Conference on Emerging Trends in Engineering*** organized by NMAM Institute of Technology, Nitte, Karnataka, pp. 258-261, May 15-16,2013.
55. **Shahana T. K.,** Babita R. Jose, Rekha K. James, K. Poulose Jacob and Sreela Sasi, "RRNS-Convolutional encoded Concatenated Code for OFDM based Wireless Communication", ***16th IEEE International Conference on Networks (ICON 2008)***, New Delhi, India, 12-14 December 2008.
56. Rekha K. James, **Shahana T.K.,** K. Poulose Jacob, Sreela Sasi, "Fixed Point Decimal Multiplication using RPS Algorithm", ***The 2008 IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA 2008),*** Sydney Australia, pp. 343-350, Dec 10 – 12, 2008.
57. Rekha K. James, **Shahana T.K**., K. Poulose Jacob, Sreela Sasi, "Decimal Multiplication using compact BCD Multiplier", ***International Conference on Electronic Design (ICED 2008),*** Penang Malaysia, Dec 1 – 3, 2008, pp. 1-6.
58. **Shahana T. K.**, Babita R. Jose, Rekha K. James, K. Poulose Jacob and Sreela Sasi, "Dual-Mode RNS based Programmable Decimation Filter for WCDMA and WLANa", ***IEEE International Symposium on Circuits and Systems (ISCAS 2008)***, Washington, USA, pp. 952-955, 18-21 May 2008.
59. **Shahana T. K.,** Babita R. Jose, Rekha K. James, K. Poulose Jacob and Sreela Sasi, "RNS based Programmable Multi-mode Decimation Filter for WCDMA and WiMAX", ***IEEE 67th Vehicular Technology Conference: VTC2008-Spring,*** Singapore, pp.1831-1835, 11–14 May 2008.
60. **Shahana T. K.,** Rekha K. James, Babita R. Jose, K. Poulose Jacob and Sreela Sasi, "Polyphase Implementation of Non-recursive Comb Decimators for Sigma-Delta A/D Converters", ***IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC 2007),*** Taiwan, pp. 825-828, 20-22 December 2007.
61. **Shahana T. K.**, Babita R. Jose, Rekha K. James, K. Poulose Jacob and Sreela Sasi, "GUI Based Decimation Filter Design Tool For Multi-Standard Wireless Transceivers", ***IET International Conference on Information and Communication Technology in Electrical Sciences (ICTES 2007)***, Chennai, India, pp. 600-605, 20-22 December 2007.

62. Babita R. J., **Shahana T. K.** and P. Mythili, "Wideband Low-Distortion Sigma-Delta ADC for WLAN with RNS based Decimation Filter", ***IET International Conference on Information and Communication Technology in Electrical Sciences (ICTES 2007)***, Chennai, India, pp. 546-552, 20-22 December 2007.
63. Rekha K. James, **Shahana T. K**, K. Poulose Jacob, Sreela Sasi, "Quick Addition of Decimals using Reversible Conservative Logic", ***15th International Conference on Advanced Computing & Communication (ADCOM 2007)***, IIT Guwahati, India, pp. 191-196, Dec 18-21, 2007**.**
64. Rekha K. James, **Shahana T. K**, K. Poulose Jacob, Sreela Sasi, "A New Look at Reversible Logic Implementation of Decimal Adder", ***The International Symposium on System-on-Chip Tampere, (SOC 2007),*** Finland, pp. 1-4, November 20-21, 2007.
65. **Shahana T. K.**, Rekha K. James, Babita R. Jose, K. Poulose Jacob and Sreela Sasi, "Performance Analysis of FIR Digital Filter Design: RNS Versus Traditional", ***7th IEEE International Symposium on Communications and Information Technologies (ISCIT 2007)***, Sydney, Australia, pp. 1-5, 16-19 October 2007.
66. Rekha K. James, **Shahana T. K**, K. Poulose Jacob, Sreela Sasi, "Fault Tolerant Error Coding and Detection using Reversible Gates", ***IEEE TENCON 2007, Taipei,*** Taiwan, pp. 1-4, Oct 30-Nov2, 2007.
67. Rekha K. James, **Shahana T. K**, K. Poulose Jacob, Sreela Sasi, "Performance Analysis of Reversible Fast Decimal Adders", WCECS International Conference on Computer Science and Applications 2007, pp. 234-239, San Francisco, USA, October 24-26, 2007, Lecture notes in Engineering and Computer Science, International Association of Engineers (IA ENG), ISBN:978-988-98671-6-4
68. Rekha K. James, **Shahana T. K**, K. Poulose Jacob, Sreela Sasi, "Improved Reversible Logic Implementation of Decimal Adder", ***11th IEEE VLSI Design And Test Symposium 2007 (VDAT 2007)***, Kolkata, India, August 8-11, 2007.
69. **Shahana T. K.**, Rekha K. James, K. Poulose Jacob, Sreela Sasi, "Genetic Algorithm-based Combinational Logic Synthesis using Universal Logic Modules", ***ESA'07 - The 2007 International Conference on Embedded Systems and Applications, WORLDCOMP 2007***, Las Vegas, Nevada, USA, pp. 210-215, 25-28 June 2007.
70. Rekha K. James, **Shahana T. K**, K. Poulose Jacob, and Sreela Sasi, "Delay-Reduced Combinational Logic Synthesis using Multiplexers", Proceedings of ***The 2006 International Conference on Embedded Systems & Applications*** – **ESA'06**, Las Vegas, Nevada, USA, pp. 105-110, June 26-29, 2006.
71. **Shahana T. K.**, Rekha K. James, Poulose Jacob, and Sreela Sasi, "Automated Synthesis of Delay-Reduced Reed-Muller Universal Logic Module Networks", ***Proceedings of 23rd IEEE Norchip Conference***, Oulu, Finland, pp. 90-93, 21-22 November 2005.

National Conferences:

72. Rijo Sebastian, Babita Roslind Jose, **Shahana T.K.,** "Low Distortion Mash ΣΔ Modulator for Digital Audio Applications", ***28th Kerala Science Congress***, pp. 1066-1071, 28-30 January 2016.
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17 February 2022 **SHAHANA T.K.**