

Workshop Report

Name of the Workshop: **5-day Hands-on Workshop/FDP on “VLSI EDA Tools for FPGA & ASIC Design”**, organized by the Department of Electronics, CUSAT, in association with MeitY under C2S Program and IEEE Kochi Subsection on December 4-8, 2023

The 5-day Hands-on Workshop/Faculty Development Program (FDP) on "VLSI EDA Tools for FPGA & ASIC Design" was a resounding success, bringing together a diverse group of 36 participants eager to delve into the intricacies of embedded systems and Application-Specific Integrated Circuit (ASIC) design. Organized by the Department of Electronics at Cochin University of Science and Technology (CUSAT) in collaboration with the Ministry of Electronics and Information Technology (MeitY) under the Chip to Startup (C2S) program, and in association with IEEE Kochi Subsection, the workshop aimed to provide a comprehensive understanding of fundamental concepts and methodologies in VLSI design.

Overview of the Workshop:

The program commenced with an inaugural talk on December 4, 2023, by Dr. Alex James, Professor Academic at Digital University Kerala. Dr. James captivated the audience with his insightful talk on "AGI Chips, the Next Frontier," exploring the transformative potential of Artificial General Intelligence (AGI) chips in the evolving landscape of VLSI design.

The subsequent two days witnessed expert hands-on sessions for FPGA conducted by Vinnalan and Shiva from CoreEL Technologies, Bengaluru. Participants gained practical insights into the Embedded Design Flow, emphasizing a hands-on approach with popular FPGA platforms such as Zedboard and Zybo boards. This interactive experience provided attendees with a holistic understanding of the development process, from conceptualization to implementation.

Technical talks on December 6 delved into crucial aspects of ASIC design. Dr. Nalesh S, Assistant Professor at the Department of Electronics, CUSAT, presented an informative session on "Introduction to ASIC Design Flow and Timing Analysis." Dr. Tripti S Warriar, also an Assistant Professor at the Department of Electronics, CUSAT, shared insights on "Verification Methodologies." Ms. Simi Sukumaran, a Research Scholar at the Department of Electronics, CUSAT, presented a compelling case study on "Application Tailored Processor Design," adding a practical dimension to the theoretical framework.

The workshop concluded with expert hands-on sessions for ASIC design on December 7th and 8th, led by Mr. Navneeth Krishna from Entuple Technologies, Bengaluru. These sessions provided participants with valuable hands-on experience in using industry-standard tools for Digital Design Flow, particularly focusing on Cadence EDA tools.

The success of this workshop would not have been possible without the collaborative efforts of the Department of Electronics at CUSAT, MeitY, IEEE Kochi Subsection, and the esteemed speakers and experts who generously shared their knowledge and expertise.

In conclusion, the 5-day Hands-on Workshop & FDP on "VLSI EDA Tools for FPGA & ASIC Design" was a resounding success, providing participants with a robust foundation in VLSI design and equipping them with practical skills essential for their professional journey in the dynamic field of embedded systems and ASIC design.

Co-ordinators,
 Dr. Tripti S Warriar & Dr. Nalesh S
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List of Participants

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