EE-9/2/2021-R&D-E
Government of India
Ministry of Electronics & Information Technology
R&D in Electronics Group
(Microelectronics Development Division)

Dated: 18.05.2023

ADMINISTRATIVE APPROVAL

Subject: Administrative Approval in respect of the project entitled "DSP and AI workload tuned Embedded RISC-V Processors" to be Implemented by Cochin University of Science and Technology (CUSAT) Kochi, PES University, Bengaluru and M/s InCore Semiconductors Private Limited, Chennai under Chips to Startup (C2S) Programme.

I am directed to refer to Administrative Approval dated 18.05.2023 for the implementation of Programme "Chips to Startup (C2S) and to convey now the approval of the Competent Authority to the implementation of the above-mentioned project at a total estimated cost of Rs. 276.41 Lakh (Rupees Two Crore Seventy Six Lakh Forty One Thousand only) Rs. 248.00 Lakh from Ministry of Electronics and Information Technology as Grant-in-Aid and Rs. 28.41 Lakh from Tectona SoftSolutions Pvt. Ltd, Ahmedabad. The duration of the project is 3 years. The details of the project are given in the enclosed **Annexure-I**.

2. This issues with the approval of Secretary, MeitY vide computer No. 3080449 dated 03.05.2023 and concurrence of JS&FA, Ministry of Electronics & Information Technology vide computer No. 3080449 dated 03.05.2023.

Meenakshi 18/5/2023

(Meenakshi Kumar)
Under Secretary

1. The Pay & Accounts Office (PAO), MeitY
2. Office of the Principal Director of Audit, Finance & Communications, Civil Lines, Near Old Secretariat, Shamnath Marg, New Delhi -110 054.
3. Prof. Tripti Warrier, Chief Investigator, Department of Electronics, Cochin University of Science and Technology (CUSAT), Kalamassery, Kochi, Kerala 682022.
4. Prof. Madhura Purnaprajna, Chief Investigator, Department of Electronics and Communication, PES University, Electronic City Campus, Near Hosur Road, Bengaluru, Karnataka-560100
5. Dr. Neel Gala, Chief Investigator, InCore Semiconductors Pvt. Ltd, No 22 (1st Floor) Tower 2, Rayala Towers, 158 Anna Salai, Chennai, Tamil Nadu- 600002
6. DG(NIELIT)/CFO(NIELIT)
7. GC(SV)/GC(AKP)/Sci. 'E'(NG)/Sci. 'D'(HG)/DS(DKS), MeitY
8. Finance Division/HRD/D&D Section, MeitY
9. Master Sanction file.

Annexure-I

1	**Name of the Project**	DSP and AI workload tuned Embedded RISC-V Processors
2	**Objective & Deliverables**	**Objective:**

The primary **objectives** of the project are to equip/enhance a base RISC-V processor with domain specific ISA (Instruction Set Architecture) extensions which can significantly improve the execution of the DSP, Cryptography and AI/ML inference workloads on IoT/5G/edge devices.

The above aim can be met by accomplishing the following:

- Designing a variety of configurable and optimized set of digital modules for three major ISA extension classes: Bit-Manipulation, Packed SIMD (Single Instruction Multiple Data) and Vector which can cater to a wide range of design points in terms of power, area and performance.
- Build a set of optimised software emulation libraries to support this extension.
- To standardizing co-processor interface protocols to integrate the implemented extensions (standard or custom) to the host RISC-V pipeline.
- An automated trace-based profiler to design an extremely tailored domain-specific RISC-V core.
- Build unit verification environment based on CoCoTb, Verilator and Python for all hardware functional blocks developed in this project.
- Integration of the above extension implementations (HW-executed or SW-emulated) with one or more RISC-V processors and prototype on FPGA to demonstrate capabilities and feasibility for end product development.
- Explore, design and architect novel micro-architectures for implementation of the integer subset in Vector ISA.
- Benchmarking applications and demonstrating benefits on modern applications.

Deliverables: -

- Re-usable HW IPs to support extensions (Bitmanip, PSIMD and Vector).
- Profiling and Verification IPs –
  - Automated trace-based profiler tailored domain-specific RISC-V core
  - Software stack to support extensions
  - Unit verification environment
- SoCs IPs with extensions and prototyped on FPGA to demonstrate capabilities

3	**Year wise Milestones**	Annexure A
4	**Name of Implementing Agencies and Legal Status**	**Lead Agency:** Cochin University of Science and Technology (CUSAT), Kochi – State University **Collaborating Agencies:** 1. PES University (PESU), Bengaluru – Private University 2. M/s InCore Semiconductors Pvt. Ltd, Chennai – Startup
5.	**Total Project Duration**	3 Years Expected date of commencement: Date of 1st release of GIA Expected date of completion: 3 Years from the date of 1st release of GIA or date of completion of C2S Programme (i.e. 10.02.2027), whichever is earlier

6. **Total Project Outlay :** **Rs. 276.41 Lakh**

MeitY Contribution: Rs. 248.00 Lakh;

Tectona SoftSolutions Pvt. Ltd Contribution: Rs. 28.41 Lakh

A. Cumulative Budget Outlay of the Project (Year wise):

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)										
	1st Year			2nd Year			3rd Year			Total	
	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry Contribution
Capital Equipment	19.04	6.34	25.38	0.00	0.00	0.00	0.00	0.00	0.00	19.04	6.34
Consumable Stores	1.50	0.00	1.50	1.50	0.00	1.50	1.00	0.00	1.00	4.00	0.00
Duty on Import	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Manpower	61.55	6.85	68.40	68.47	7.61	76.08	68.47	7.61	76.08	198.49	22.07
Travel & Training	6.00	0.00	6.00	6.00	0.00	6.00	6.00	0.00	6.00	18.00	0.00
Contingencies	2.00	0.00	2.00	2.00	0.00	2.00	2.00	0.00	2.00	6.00	0.00
Overheads, if any	0.91	0.00	0.91	0.78	0.00	0.78	0.78	0.00	0.78	2.47	0.00
Grand Total	**91.00**	**13.19**	**104.19**	**78.75**	**7.61**	**86.36**	**78.25**	**7.61**	**85.86**	**248.00**	**28.41**

B. Agency wise Budget Outlay (Year Wise):

❖ Cochin University of Science and Technology Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)										
	1st Year			2nd Year			3rd Year			Total	
	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry Contribution
Capital Equipment	9.52	3.17	12.69	0.00	0.00	0.00	0.00	0.00	0.00	9.52	3.17
Consumable Stores	0.75	0.00	0.75	0.75	0.00	0.75	0.50	0.00	0.50	2.00	0.00
Duty on Import	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Manpower	16.09	1.79	17.88	16.09	1.79	17.88	16.09	1.79	17.88	48.27	5.37
Travel & Training	2.00	0.00	2.00	2.00	0.00	2.00	2.00	0.00	2.00	6.00	0.00
Contingencies	1.00	0.00	1.00	1.00	0.00	1.00	1.00	0.00	1.00	3.00	0.00
Overheads, if any	0.30	0.00	0.30	0.20	0.00	0.20	0.20	0.00	0.20	0.70	0.00
Grand Total	**29.66**	**4.96**	**34.62**	**20.04**	**1.79**	**21.83**	**19.79**	**1.79**	**21.58**	**69.49**	**8.54**

❖ PES University Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)										
	1st Year			2nd Year			3rd Year			Total	
	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry Contribution
Capital Equipment	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Consumable Stores	0.75	0.00	0.75	0.75	0.00	0.75	0.50	0.00	0.50	2.00	0.00
Duty on Import	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Manpower	8.96	1.00	9.96	13.18	1.46	14.64	13.18	1.46	14.64	35.32	3.92
Travel & Training	2.00	0.00	2.00	2.00	0.00	2.00	2.00	0.00	2.00	6.00	0.00
Contingencies	1.00	0.00	1.00	1.00	0.00	1.00	1.00	0.00	1.00	3.00	0.00
Overheads, if any	0.13	0.00	0.13	0.17	0.00	0.17	0.17	0.00	0.17	0.47	0.00
Grand Total	**12.84**	**1.00**	**13.84**	**17.10**	**1.46**	**18.56**	**16.85**	**1.46**	**18.31**	**46.79**	**3.92**

❖ InCore Semiconductors Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)										
	1st Year			2nd Year			3rd Year			Total	
	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry/ End-User Contribution	Total	MeitY Contribution	Industry Contribution
Capital Equipment	9.52	3.17	12.69	0.00	0.00	0.00	0.00	0.00	0.00	9.52	3.17
Consumable Stores	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Duty on Import	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Manpower	36.50	4.06	40.56	39.20	4.36	43.56	39.20	4.36	43.56	114.90	12.78
Travel & Training	2.00	0.00	2.00	2.00	0.00	2.00	2.00	0.00	2.00	6.00	0.00
Contingencies	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Overheads, if any	0.48	0.00	0.48	0.41	0.00	0.41	0.41	0.00	0.41	1.30	0.00
Grand Total	**48.50**	**7.23**	**55.73**	**41.61**	**4.36**	**45.97**	**41.61**	**4.36**	**45.97**	**131.72**	**15.95**

7. Implementation Modalities : Cochin University of Science and Technology (CUSAT), Kochi as Lead Agency is responsible for overall implementation of the Project.

8. Mode and extent of funding : **As indicated below:**

(i) Budgetary Support

(a) Grants-in-aid : Rs. 248.00 Lakh (MeitY)
(b) Loan : NIL

(ii) Internal generation : NIL

(iii) External Agency, if any : Rs. 28.41 Lakh (Tectona SoftSolutions Pvt. Ltd)

9. Stages of release

Release No.	Pre-condition/ Stages	Documentation to be supplied by Implementation Agency	Amount to be released
1st release	Initiation of the project	Acceptance of Terms and Conditions governing Grants-in-aid.	Rs. 29.66 Lakh (CUSAT)
			Rs. 12.84 Lakh (PESU)
			Rs. 48.50 Lakh (M/s Incore Semiconductors Pvt. Ltd.)

Meenakshi

2nd and subsequent releases	Recommendations of the PRSG & satisfactory progress report of the project	a) Submission of Utilization Certificate of the previous release. b) Technical & Financial Progress Report. **c)** Audited Statement of Accounts (at the time of Project Closure).	Rs. 39.83 Lakh (CUSAT)
			Rs. 33.95 Lakh (PESU)
			Rs. 83.22 Lakh (M/s Incore Semiconductors Pvt. Ltd.)
		Total	**Rs. 248.00 Lakh**

Meenakshi

(Meenakshi Kumar)
Under Secretary

Year-wise deliverables/Outcomes with specific intermediate milestones (in terms of aims and objectives)

In this project InCore Semiconductors Pvt Ltd. provides the necessary lead architect and verification lead, and thus majority of the responsibilities are shared between InCore and the respective Academic Institute.

Sl. No.	Quarterly Milestones	Timelines (months)	Outcomes	Responsible Institutes
1	Hardware design for bit manipulation feature	0-4	Bit manipulation hardware and emulation routine	Incore and CUSAT
2	Emulation routine design for bit manipulation	0-3		
3	Integration and testing of core with hardware/Software bit manipulation feature	4-7	Core with bit manipulation extension	Incore and CUSAT
4	Verification of bit manipulation hardware as standalone unit	4-6	Verified Bit manipulation hardware	Incore and CUSAT
5	FPGA implementation core with bit manipulation instruction support	8-10		Incore and CUSAT
6	Validation of bit manipulation software	7-9		Incore and CUSAT
7	Modifying the compiler to include bit manipulation instructions set	4-9	Compiler with bit manipulation support	CUSAT
8	Performance evaluation of the system with bit manipulation instruction set	10-12		Incore and CUSAT
9	Hardware design for P-SIMD instruction set	10-15		Incore and CUSAT
10	Emulation routine design for P-SIMD instruction set	13-18		Incore and CUSAT
11	Integration and testing of core with hardware/Software vector feature	16-17	Core with P-SIMD extension	Incore and CUSAT
12	Verification of P-SIMD hardware as standalone unit	12-17	Verified P-SIMD hardware	Incore and CUSAT
13	FPGA implementation core with P-SIMD instruction support	17-18		Incore and CUSAT
14	Validation of P-SIMD software	16-20		Incore and CUSAT
15	Modifying the compiler to include P-SIMD instructions set	10-16	Compiler with P-SIMD Support	CUSAT
16	Performance evaluation of the system with P-SIMD instructions	20-23		Incore and CUSAT
17	Cycle accurate performance model of BitManip and P-SIMD instructions	13-15		Incore and PESU

18	Subset identification	16-18		Incore and PESU
19	Integration into microarchitecture	19-21		Incore and PESU
20	Integration into compiler	22-14	Application profiler	Incore and PESU
21	Benchmark of applications on Base RISCV ISA	0-3		PESU
22	Analysis and survey of existing RISC-V micro-architectures	7-9		PESU
23	Design of Micro-Architecture for Vector	10-15		Incore and PESU
24	HW implementation of micro-architecture	16-24	Core with vector support	Incore and PESU
25	Verification of Micro Architecture	25-33		Incore and PESU
26	Benchmarking and Further optimizations	29-36		Incore and PESU
27	Compiler work	23-28	Compiler for Vector Extension	PESU